A New 8V – 60V rated Low Vgs NLDMOS Structure with Enhanced Specific on-Resistance

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Abstract — We present a new 0.35um BCDMOS technology with a capability of 8 to 60V NLDMOS. The proposed process do not need level shifter, charge pump and boost up due to the same gate oxide thickness with logic 5V CMOS. And the Rsp of the proposed 24V NLDMOS structure is lower by 46% than conventional structure. The process has no thermal budget modification but use simple additional implant step. Also it is compatible with the conventional BCDMOS. The power LDMOS transistors in the process have very competitive performances with NLDMOS in 0.15 – 0.25um BCDMOS technologies.

I. INTRODUCTION

Recently, BCDMOS(Bipolar–CMOS–LDMOS) process is widely used in variety of areas such like LED Driver, Panel Bias IC, Switching Regulator, Battery IC, Audio Amplifier, Motor Drivers, large displays (TV and monitor), Power Management products, and storage controller chips[1-5]. Generally, the gate voltage of high voltage NLDMOS is different from a logic CMOS so that function blocks(level shifter, charge pump, boost up) is needed. However, that increases chip size and provides limitation in consumer and mobile Power IC products. And the conventional NLDMOS structure in 0.15-0.25um technologies has limitation in improving Rsp(Specific on-resistance) due to STI(Shallow Trench Isolation). Therefore, we present the new NLDMOS structures in 0.35um BCDMOS process. The gate voltage level of the proposed NLDMOS is same with that of 5V CMOS so that Function Blocks for level shifter are not needed. And the Rsp of the proposed 24V NLDMOS structure is lower by 46% than conventional one. The proposed LDMOS transistors in 0.35um BCDMOS have very competitive Rsp compared to 0.15-0.25um BCDMOS process. These advantages can dramatically reduce chip size. The proposed process simply used an additional mask for implant and the thermal budget is identical to the original 0.35um BCD process. Therefore, a logic CMOS and all the other components are compatible in the proposed process.

II. DEVICE STRUCTURE AND OPERATION

The proposed LDMOS transistors have gate oxide of 5V/125Å and were fabricated in 0.35um BCDMOS. The original process features two gate oxide of 5V/125Å and 12V/300Å for 5V CMOS and LDMOS transistors, respectively. The proposed process has only one additional mask to perform MV-NWELL and HV-PWELL. The
additional implant for both MV-NWELL and HV-PWELL is driven in by the same annealing process of the original HV-NWELL. Fig.1 shows the proposed LDMOS and conventional one. And both transistors have same gate oxide thickness. As shown in Fig. 1, MV-NWELL of the proposed low voltage (8~12V) NLDMOS fully overlaps HV-NWELL to reduce Rsp. The proposed medium voltage (18~40V) NLDMOS transistors have a lower Rsp due to highly doped MV-NWELL. As shown in Fig. 1, MV-NWELL of the proposed low voltage (8~12V) NLDMOS fully overlaps HV-NWELL to reduce Rsp. The proposed medium voltage (18~40V) NLDMOS transistors have a lower Rsp due to highly doped MV-NWELL. Shallow MV-NWELL and deep HV-PWELL are designed to achieve medium breakdown voltage of 58V. NWELL is formed by same mask step of 5V NMOS body[1]. Also the proposed high voltage (50~60V) NLDMOS has a lower Rsp because MV-NWELL has a higher doping concentration than HV-NWELL. We made a gap(HV-PWELL) between the HV-NWELL and the source to ensure high breakdown voltage. The gap releases the electric field crowding between the p-body and NBL[2]. Fig. 2 shows the simulated device net doping concentration and potential distribution at breakdown. The space between the potential lines is 1V. As shown in Fig. 2(b), the depletion region of the proposed 50V NLDMOS between p-body and NBL is more wide than that of the conventional one at VDS=70V. Fig.3 and Fig. 4 shows net doping concentration and electric field on the surface of the NLDMOS transistors.
respectively. The BVdss of the proposed transistor is equal to that of conventional one. As shown in Fig. 3(a) and 3(b), the proposed LDMOS has higher doping concentration than conventional one in drift. However, both devices are showing similar electric field near gate edge and n+ drain in Fig 4(a) and Fig. 4(b). Therefore, the proposed structures have enhanced Rsp and ensure high breakdown voltage.

III. EXPERIMENTAL RESULT

Fig. 5 shows that the forward \( I_{DS} - V_{DS} \) characteristics for the 40V high-side and low-side LDMOS transistors and the device shows good performance up to \( V_{GS} = 5\mathrm{V} \), \( V_{DS} = 40\mathrm{V} \). The characteristics of the breakdown voltage and the specific on-resistance are shown in Fig. 6. The proposed NLDMOS and conventional one have the same 125 Å oxide thickness for performance comparison. The Rsp of the proposed 24V NLDMOS structure is lower by 46% than conventional one at BVdss=32V. Those results demonstrate that the proposed structures can enhance Rsp dramatically. Fig. 7 plots the NLDMOS Rsp vs. BVdss for the proposed process and 0.15-0.25um BCDMOS technologies. The maximum available gate voltage of NLDMOS for different technologies is \( V_{GS} = 3.3\mathrm{V} \) or 5V. The proposed LDMOS shows good performance compared to the 0.15-0.25um BCDMOS technologies. Especially, at the high voltage ranges (50~60V), the devices show better BVdss vs Rsp performance than different technologies. Fig.8 shows the long term SOA (safe operating area) of the proposed 50V high-side LDMOS and the device is safe in 100% duty cycle.
Fig. 6. Comparison of N-LDMOS Rsp vs. BVdss figure of merit for the proposed NLDMOS and conventional one.

Fig. 7. Benchmark of NLDMOS Rsp vs. BVdss for the 0.15-0.25um BCDMOS.

IV. CONCLUSION

In this paper, we developed a new 0.35um BCDMOS technology with a capability of 8 to 60V NLDMOS. The proposed LDMOS has the same gate oxide thickness with logic 5V CMOS. And MV-NWELL and HV-PWELL are employed to ensure high breakdown voltage and low on-resistance. The proposed process has no thermal budget modification but uses simple additional implant step. Also it is compatible with the conventional BCDMOS. Furthermore, the power LDMOS transistors in the process have competitive performances with NLDMOS in 0.15 – 0.25um BCDMOS technologies.

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REFERENCES